UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,121	02/13/2002	Thomas Bolt	Q02-1031-US1	7279

7590 08/10/2005

Robert A Saltzberg
MORRISON & FOERSTER LLP
425 Market Street
San Francisco, CA 94105

EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,121	BOLT ET AL.	
	Examiner	Art Unit	
	Nimesh G. Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *28-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 3, 5-10, 12-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al.(2002/0081873), in view of Talati('402).

4. Regarding claim 1, Harris discloses a USB system for data communication between a processor and IDE devices, comprising: an IDE device(Fig 2, 20); a USB-to-IDE bridge(Figure 2, 25), wherein the IDE device is connected to a respective USB-to-IDE bridge; and a USB controller(It is inherent the host has a USB controller in a USB system), wherein the USB-to-IDE bridge is connected to the USB controller via a USB bus, each USB-to-IDE bridge providing protocol conversion for communication between the corresponding IDE device and the USB controller, whereby the processor can communicate with the IDE devices via the USB controller(Paragraph 9).

Harris does not specifically disclose a plurality of IDE devices and plurality of USB-to-IDE bridges, wherein each IDE device is connected to a respective USB-to-IDE bridge. However, Talati discloses plurality of bridges to connect plurality of IDE devices(Figure 1). Therefore, it would have been

obvious to use plurality of IDE-to-USB bridges connected to a respective IDE device since this would enable multiple IDE devices to be connected to the host using the USB interface and increase storage capacity. Further, it has been held that mere duplication of the essential working parts of said USB-to-IDE bridge, which is coupled to an IDE device, involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.*

5. Regarding claim 3, Harris and Talati disclose a system, further comprising one or more USB hubs(Talati; Figure 1, 102, 104), each USB hub connected between two or more USB-to-IDE bridges and a USB controller(It is inherent in USB system that USB controller is in the Host).

6. Regarding claim 5, Harris discloses a system, wherein one or more IDE devices can be connected/disconnected to/from the system while the system is operating(Paragraph 25).

7. Regarding claim 6, Harris and Talati disclose a system, wherein at least a third IDE device coupled to a corresponding USB-to-IDE bridge can be connected to the USB controller while the system is operating(Paragraph 25).

8. Regarding claim 7, Harris and Talati disclose a system, further comprising at least one USB hub(Talati; Figure 1, 102, 104) connected between a number of the USB-to-IDE bridges and the USB controller(It is inherent in USB system that USB controller is in the Host), whereby the processor can communicate with the IDE devices via the USB controller and the USB hub.

9. Regarding claim 8, Harris and Talati disclose a system, wherein one or more IDE devices can be disconnected from the system while the system is operating(Paragraph 25).

10. Regarding claim 9, Harris and Talati disclose a system, wherein at least one additional IDE device coupled to a corresponding USB-to-IDE bridge can be connected to the USB hub while the system is operating(Paragraph 25).

11. Regarding claim 10, Harris discloses a method for connecting a IDE device(Fig 2, 20) to a processor for data communication, comprising the steps of: providing a USB-to-IDE bridge(Figure 2, 25);

connecting the IDE device to the USB-to-IDE bridge; providing a USB controller(It is inherent the host has a USB controller in a USB system); and connecting the USB-to-IDE bridge to the USB controller via a USB bus, each USB-to-IDE bridge providing protocol conversion for communication between the corresponding IDE device and the USB controller, whereby the processor can communicate with the IDE devices via the USB controller(Paragraph 9.

Harris does not specifically disclose a plurality of IDE devices and plurality of USB-to-IDE bridges, wherein each IDE device is connected to a respective USB-to-IDE bridge. However, Talati discloses plurality of bridges to connect plurality of IDE devices(Figure 1). Therefore, it would have been obvious to use plurality of IDE-to-USB bridges connected to a respective IDE device since this would enable multiple IDE devices to be connected to the host using the USB interface and increase storage capacity. Further, it has been held that mere duplication of the essential working parts of said USB-to-IDE bridge, which is coupled to an IDE device, involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.*

12. Regarding claim 12, Harris and Talati disclose a method, further comprising the steps of hot plugging/unplugging one or more IDE devices to/from the USB-to-IDE bridges(Paragraph 25).

13. Regarding claim 13, Harris and Talati disclose a method, wherein one or more IDE devices can be connected/disconnected to/from the system while the system is operating(Paragraph 25).

14. Regarding claim 14, Harris and Talati disclose a method, wherein at least a third IDE device coupled to a corresponding USB-to-IDE bridge can be connected/disconnected to/from the USB controller while the system is operating(Paragraph 25).

15. Regarding claim 15, Harris and Talati disclose a method, further comprising the steps of providing at least one USB hub(Talati; Figure 1, 102, 104); connecting each hub to a USB controller(It is inherent in USB system that USB controller is in the Host); and connecting two or more USB-to-IDE

bridges to each hub, such that each hub is connected between a USB controller and two or more USB-to-IDE bridges.

16. Regarding claim 16, Harris and Talati disclose a method, further comprising the steps of disconnecting one or more of the IDE devices from the system while the system is operating(Paragraph 25).

17. Regarding claim 17, Harris and Talati disclose a method, further comprising the steps of connecting at least one additional IDE device coupled to a corresponding USB-to-IDE bridge, to one of the hubs while the system is operating(Paragraph 25).

18. Regarding claim 18, Harris discloses a data storage system, comprising: an IDE device(Fig 2, 20); a USB-to-IDE bridge(Figure 2, 25), wherein the IDE device is connected to a respective USB-to-IDE bridge; and a USB controller(It is inherent the host has a USB controller in a USB system), wherein the USB-to-IDE bridge is connected to the USB controller via a USB bus, each USB-to-IDE bridge providing protocol conversion for communication between the corresponding IDE device and the USB controller, whereby the processor can communicate with the IDE devices via the USB controller(Paragraph 9).

Harris does not specifically disclose a plurality of IDE devices and plurality of USB-to-IDE bridges, wherein each IDE device is connected to a respective USB-to-IDE bridge. However, Talati discloses plurality of bridges to connect plurality of IDE devices(Figure 1). Therefore, it would have been obvious to use plurality of IDE-to-USB bridges connected to a respective IDE device since this would enable multiple IDE devices to be connected to the host using the USB interface and increase storage capacity. Further, it has been held that mere duplication of the essential working parts of said USB-to-IDE bridge, which is coupled to an IDE device, involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.*

19. Regarding claim 19, Harris discloses a data storage system, further comprising a carrier for each IDE data storage device, such that each IDE disk drive and corresponding USB-to-IDE bridge are stored in the respective carrier(Figure 3).

20. Regarding claim 20, Harris and Talati disclose a system, wherein one or more IDE devices can be disconnected from the system while the system is operating(Paragraph 25).

21. Regarding claim 21, Harris and Talati disclose a system, wherein at least a third IDE device coupled to a corresponding USB-to-IDE bridge can be connected to the USB hub while the system is operating(Paragraph 25).

22. Regarding claim 22, Regarding claim 7, Harris and Talati disclose a system, further comprising at least one USB hub(Talati; Figure 1, 102, 104) connected between a number of the USB-to-IDE bridges and the USB controller(It is inherent in USB system that USB controller is in the Host), whereby the processor can communicate with the IDE devices via the USB controller and the USB hub.

23. Regarding claim 23, Harris and Talati disclose a system, further comprising one or more USB hubs(Talati; Figure 1, 102, 104), each USB hub connected between two or more USB-to-IDE bridges and a USB controller(It is inherent in USB system that USB controller is in the Host).

24. Regarding claim 24, Harris and Talati disclose a system, wherein one or more IDE storage devices can be disconnected from the system while the system is operating(Paragraph 25).

25. Regarding claim 25, Harris and Talati disclose a system, wherein at least one additional IDE storage device coupled to a corresponding USB-to-IDE bridge can be connected to one of the USB hubs while the system is operating(Paragraph 25).

26. Regarding claim 26, Harris and Talati disclose a system, wherein at least one additional IDE device coupled to a corresponding USB-to-IDE bridge and associated hub can be connected to the USB hub while the system is operating(Paragraph 25).

27. Regarding claim 27, Harris and Talati disclose a system, wherein at least one IDE device coupled to a corresponding USB-to-IDE bridge and associated hub can be disconnected from the USB controller while the system is operating(Paragraph 25).

28. Claims 2 and 4, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris, in view of Talati('402), and in further view of Abramson et al.('135).

29. Regarding claim 2, Harris and Talati do not specifically disclose the USB controller is connected to the processor via a PCI bus. However, Abramson discloses the USB controller connected a processor via PCI bus(Figure 1). Therefore it would have been obvious to one of ordinary skill in the art to use a PCI bus to connect the USB controller to the processor since PCI bus is the most common bus used in modern day computer.

30. Regarding claim 4, Harris discloses one or more USB-to-IDE bridges are connected to each USB controller via a USB bus, each USB-to-IDE bridge providing protocol conversion for communication between the corresponding IDE device and that USB controller, whereby the processor can communicate with the IDE devices via the USB controllers(Paragraph 9).

Harris and Talati do not specifically disclose a plurality of USB controllers connected to the processor. However Abraham discloses a plurality of USB controllers connected to the processor(Figure 1). Therefore it would have been obvious use a plurality of USB controllers in the system of Harris and Talati since this would improve bandwidth(Column 1, Lines 46-50).

31. Regarding claim 11, Harris and Talati do not specifically disclose the USB controller is connected to the processor via a PCI bus. However, Abramson discloses the USB controller connected a processor via PCI bus(Figure 1). Therefore it would have been obvious to one of ordinary skill in the art to use a PCI bus to connect the USB controller to the processor since PCI bus is the most common bus used in modern day computer.

Response to Arguments

32. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP
August 6, 2005

TIM VO
PRIMARY EXAMINER